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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,321	03/06/2002	Makoto Kanbe	1035-371	7734

7590 01/29/2003

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EXAMINER	
NGUYEN, JIMMY H	
ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 01/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	10/091,321	KANBE ET AL.	
	Examiner	Art Unit	
	Jimmy H. Nguyen	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18,20,23,31,33,40,41 and 45-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18,20,23,31,33,40,41 and 45-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *08/974,496* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6,9* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This Office Action is made in response to applicant's papers filed on 03/06/02. Claims 18, 20, 23, 31, 33, 40, 41 and 45-49 are currently pending in the application. However, claim 23 depends on the cancelled claim 19; therefore, this claim should be cancelled. An action follows below:

Information Disclosure Statement

2. The information disclosure statements (IDS) submitted on 03/06/02 and 07/03/02 and respectively entered as paper No. 6 and 9 are considered by the examiner. However, the Japanese reference, 170986/1989, cited in the IDS filed on 03/06/02, is crossed out because it is also cited in the IDS filed 07/03/02.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the features, "power source OFF detecting means, panel power maintaining means and erasing means including a source driver control circuit and an opposing electrode control circuit" as recited in claim 18, "power source OFF detecting means, panel power maintaining means and erasing means for applying rectangular wave signal to opposing electrode" as recited in claim 49, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

The application, especially in the first group including the first to fourth embodiments as illustrated in figures 1-12, discloses the power source OFF detecting means and panel power maintaining means, as recited in independent claims 18 and 49, and especially in the second group including the fifth to seventh embodiments as illustrated in figures 15-30, further discloses erasing means and opposing electrode, as recited in independent claims 18 and 49. However, a combination of these two groups (i.e., independent claims 18 and 49) (i.e., the erasing device comprising the power source OFF detecting means and panel power maintaining means of the first group, and erasing means and opposing electrode of the second group) is not described expressly in the application.

It is suggested that the claimed features, "power source OFF detecting means and panel power maintaining means" as recited in independent claims 18 and 49, should be changed to the "power source OFF detecting means and panel power maintaining means" as similarly recited in independent claim 40, lines 6-10, **so as to overcome the objections to the specification and the drawings above, and to make the instant application fully entitled to the benefit of the filing date of the parent application**. It is in the best interest of the patent community that applicant, in his/her normal review and/or rewriting of the claims, to take into consideration these editorial situations and make changes as necessary.

Claim Objections

5. Claim 18 is objected to because of the following informalities: line 7, "the main" should be changed to -- the power source of the main --, so as to be consistent with the specification, page 7, lines 21-23. Appropriate correction is required.

6. Claim 46 is objected to because of the following informalities: line 7, -- circuit -- should be inserted immediately after "control", so as to be consistent with the limitation in line 5. Appropriate correction is required.

7. Claim 49 is objected to because of the following informalities: line 6, "the main" should be changed to -- the power source of the main --, so as to be consistent with the specification, page 7, lines 21-23. Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 40 and 41 are rejected under 35 U.S.C. 102(b) as being anticipated by Yasui et al. (USPN: 5,248,963, cited in IDS filed on 03/06/02), hereinafter Yasui.

As per claims above, the claimed invention reads on Yasui as follows: Yasui discloses an erasing device for a liquid crystal display (LCD) image, provided in a LCD device (see fig. 3) having a LCD panel (10) whose pixels are driven by active elements (TFTs 13), for erasing a display image on said LCD panel when a power source of a main body of said LCD device is turned off, comprising power source OFF detecting means (a voltage drop detector 24) for detecting whether the power source of the main body of LCD device is turned off (fig. 5, col. 5,

lines 8-30), panel power maintaining means (a power holding circuit 22) for supplying power to said LCD panel for a certain period when said power source OFF detecting means detects said OFF signal, and erasing means (23, 25, 27, 17 and 16) for applying to all pixels in the LCD panel with an OFF-level voltage (a voltage level corresponding to pixel data D of logic "0", col. 4, lines 5-16), using the power supplied by said panel power maintaining means. Yasui further teaches erasing means outputting a gate driving signal (a clear signal CL), which turns on gate lines (G1-Gm) sequentially to turn on the active elements (TFTs 13) per line by means of a gate driver (a gate bus driver 19) (see figs. 2 and 4), and outputting a voltage signal (E2) to both pixel electrode (12a) and opposing electrode (12b), by means of the source driver (source bus drive circuit 16) and the inherent opposing electrode signal control circuit (fig. 3, col. 3, lines 58-67). The elements in the claims are read in the reference.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 18, 20, 23, 31, 33 and 45-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasui in view of Hayashi (USPN: 5,313,282, cited in IDS filed on 03/06/02).

Regarding to claims 18, 23 and 49, Yasui discloses an erasing device for a liquid crystal display (LCD) device (fig. 3) having a LCD panel (10) whose pixels are driven by active elements (13), for erasing a display image on said LCD panel when a power source of a main body of said LCD device is turned off, comprising power source OFF detecting means (a voltage

drop detector 24) for detecting a signal (V1) and for outputting an OFF signal (output V_B) (see fig. 5), panel power maintaining means (a power holding circuit 22) for supplying power to said LCD panel for a certain period, and erasing means (23, 25, 27, 17 and 16) for applying an OFF-level voltage (a voltage level corresponding to pixel data D of logic "0", col. 3, lines 58-60), using the power supplied by said panel power maintaining means, to all pixels in said LCD panel, thereby erasing the display in a short time after the turning OFF of the power supply (figs. 3 and 5, col. 3, lines 1-22 and lines 58-67). Yasui further discloses the erasing means including a source driver (a source bus driver 16), an inherent source driver control circuit for providing signals (D, PCK and M) to control the source driver (fig. 3) and an inherent opposing electrode control circuit for outputting an opposing electrode signal (a voltage signal E2) to opposing electrodes (common electrodes 12b) (fig. 3, col. 3, lines 58-67), so that the pixel electrode and the opposing electrode receive an OFF voltage (E2) that turns OFF a liquid crystal (col. 3, line 58 through col. 4, line 16). Accordingly, Yasui discloses the claimed subject matter except that Yasui does not disclose expressly a detected signal that instructs to turn OFF the power source of the main body of said LCD device.

However, Hayashi teaches a method and an apparatus in the display device for controlling the power source of the main body of display device, wherein the display device includes a detector (19) for receiving an OFF signal command from a user input device (20) and a micro-computer for detecting an OFF signal that instruct to turn OFF the power source of the main body of the display device (figure 1, abstract). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to utilize Hayashi's teaching in the LCD device of Yasui because this would allow a user to control the electrical power supplying to

a display device, as taught by Hayashi (see abstract). Therefore, it would have been obvious to combine Hayashi with Yasui to obtain the invention as specified in claims above.

Regarding to claims 20 and 45, Yasui further discloses that the erasing means applies to all pixels the OFF-level voltage by providing the same rectangular wave signal (i.e., the rectangular wave signal having an amplitude of E2) to both the pixel electrode and the opposing electrode (col. 3, line 58 through col. 4, line 16). Therefore, these claims are rejected for the reason above.

Regarding to claims 31 and 33, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to recognize the active matrix type LCD device of Yasui including a reflective LCD device and a Guest-Host LCD device. Therefore, these claims are rejected for the reason above.

Regarding to claims 46 and 47, Yasui discloses the erasing means further including a gate driver (a gate bus driver 19) and a gate driver control circuit (a circuit including elements 18 and 20) (see fig. 4). Yasui further teaches erasing means outputting a gate enable signal (a clear signal CL), as a starting signal for the gate driver, into the gate driver control circuit, so that a gate signal is outputted to gate lines (G1-Gm) (see figs. 2 and 4). Therefore, these claims are rejected for the reason above.

Regarding to claim 48, Yasui further discloses that, during the erasing period (T), the gate signal is fixed at a high level (col. 4, lines 3-11). Therefore, this claim is rejected for the reason above.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The references, Kanatani et al (USPN: 5,412,397, see figs. 1 and 4, col. 5, lines 37-50) and Moon (USPN: 5,793,346, see fig. 4, abstract), both teach related LCD device having an erasing means for eliminating a residual image when the power is turned off.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy H. Nguyen whose telephone number is (703) 306-5422. The examiner can normally be reached on Monday - Thursday, 8:00 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached at (703) 305-4938.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

JHN
January 27, 2003

BIPIN SHALWALA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600